SECTION 1

SCOPE

This document describes the functional, environmental, mechanical, and quality requirements for the Mapper to be used on the TI 99/8 Personal Computer.

SECTION 2

APPLICABLE DOCUMENTS

* TI 99/8 Personal Computer.
* TMS9900 16-bit microprocessor.
* TMS9995 16-bit microprocessor.

SECTION 3

FUNCTIONAL SPECIFICATION

3.1 FUNCTIONAL DESCRIPTION

The Mapper is a device used to extend the 16-bit Logical Address Space (LAS) of the TMS9995 Microprocessor to a 24-bit Physical Address Space (PAS). Additional functions are noted in the following paragraphs.

As the TI 99/8 Personal Computer is organized to have some memory mapped devices connected in the LAS, not all memory access will go through the Mapper. If a memory operation is not currently occuring, a Communications Register Unit (CRU) MIGHT be; therefore, the LAS must pass straight through the Mapper in that case.

The Mapper shall be a 5V only part, and be a TTL compatible part.

3.1.1 LAS-PAS Operation. The Mapper is to contain sixteen 27-bit registers or memory locations to provide a 24-bit address base and three protect bits for mapping sixteen 4K LAS pages to 4K contigous blocks in the PAS.

The four Most Significant Bits (MSB) of the TMS9995 Microprocessor Address Bus select which of the sixteen base registers is to be used, and the remaining twelve bits of the TMS9995 Address Bus forms a displacement which is to be added (within the Mapper) to the 24 bit address base to form the effective 24-bit PAS.

The base register access and the addition time occur during the first clock cycle of the TMS9995 memory access. This operation is described in a subsequent paragraph.

The LAS Address Bus shall be passed through the Mapper if a PAS memory cycle is not occuring to satisfy possible Communication Register Unit (CRU) operation, and to enhance testing characteristics.

3.1.2 PAS Memory Control Signals. The Mapper shall generate signals similiar to those of the TMS9900 for PAS memory cycle control to futher preserve compatibility of existing TI Personal Computer Peripherals.

3.1.2.1 MEMEN*. The first clock cycle of the TMS9995 memory access shall be suppressed from the PAS to allow for base register access and adder settling time. The mapper shall generate a signal timed the same as the TMS9995 MEMEN* one clock period later, and this signal (PMEMEN*) shall last two more clock cycles if the System READY status signal is in the HIGH (TRUE) state. If READY is not TRUE, the length of PMEMEN* shall be determined by READY. As this indicates, a minimum PAS memory cycle consists of three TMS9995 clock periods even though PMEMEN* has only two clock periods. The third period is lost in base register access and adder settling time.

3.1.2.2 Address MUX. The address is multiplexed in order to conserve both cable wires and package pins. A control signal, Most Significant Address Strobe (MSAST*), shall be generated to indicate when the Most Significant 8-bits of the 24-bit PAS is stable. These eight bits are formatted on the Least Significant BYTE (LSBY) of the Mapper address bus. The MSBY of this word is comprised of the three protect bits and five logic zeros.

It shall be the responsibility of the user to clock this BYTE into a register on the falling edge of MSAST*. MSAST* shall occur somewhere within the first clock period of the three clock period minimum cycle. The Most Significant 8-bits of the Mapper address bus shall contain the three protect bits and five zeros. For additional information, see the paragraph on maper address bus formatting.

3.1.2.3 PH3*. The Mapper shall modify the TMS9995 CLKOUT clock from the current 50% duty cycle to one of a 25% LOW signal (PH3*) to resemble that of a TMI9904A Clock Generator. The falling edge of PH3* shall correspond to the rising edge of the TMS9995 CLKOUT signal.

3.1.2.4 DBIN. The memory data bus direction control signal DBIN* of the TMS9995 shall be modified to the timing of that of the TMS9900 prior to the time that PMEMEN* occurs. The TMS9995 DBIN* shall be invered and passed through the Mapper if a PAS memory cycle is not occuring.

3.1.2.5 WE*. The memory Write Enable/CRU CLOCK control signal of the TMS9995 shall be decoded and generated by the mapper for PAS cycles only. It shall remain HIGH for all LAS cycles.

3.2 MAPPER LOADING

The Mapper Control and Status registers shall be located on the LAS side of the Mapper, and the mapper shall be loaded upon command from the TMS9995. Once initiated, a 64 BYTE burst transfer shall occur from the 2K Static RAM (SRAM) in the TI 99/8 to the Mapper. The TMS9995 shall be placed in the HOLD state for this operation.

A Move BYTE operation from the TMS9995 to the Mapper shall initiate this burst transfer. The Mapper response address is >8810 if CRUS=HIGH, and >F870 if CRUS=LOW. The 64 BYTEs shall come from any one of eight different base locations in the SRAM, and the BYTE of data moved into the Mapper shall determine which one. The format is as follows.

MSB LSB	
0000 xxx1	xxx is the block within the SRAM. These blocks start at the zero end of the SRAM, and are based at >40 increments, and the MSBY is based at zero.

3.3 MAPPER SAVING

The mapper shall be saved upon command from the TMS9995. Once initiated, a 64 BYTE burst transfer shall occur to the 2K Static RAM (SRAM) in the TI 99/8 from the Mapper. The TMS9995 shall be placed in the HOLD state for this operation.

A Move BYTE operation from the TMS9995 to the Mapper shall initiate this burst transfer. The Mapper response address is >8810 if CRUS=HIGH, and >F870 if CRUS=LOW. The 64 BYTEs shall go to any one of eight different base locations in the SRAM, and the BYTE of data moved into the Mapper shall determine which one. The format is as follows.

MSB LSB	
0000 xxx0	xxx is the block within the SRAM. These blocks start at the zero end of the SRAM, and are based at >40 increments, and the MSBY is based at zero.

3.4 PROTECT FEATURES

Each 4K LAS block may be protected for any combination of three conditions.

* WRITE Protect- If this bit is HIGH, no WRITE is allowed in this area. Hardware is to inhibit a WRITE operation, Set a WRITE Protect violation bit, and create an interrupt to the TMS9995.

* EXECUTE Protect- If this bit is HIGH, an instruction execute shall not be legal in this area. Hardware is to Set an Execute Protect violation bit, and create an interrupt to the TMS9995. The instruction may or may not execute depending on the pipelining in the TMS9995, and the Mapper is not to attempt to alter the normal course of events.

* READ Protect- If this bit is HIGH, no DATA READ (Instruction Fetch is valid though) is allowed in this area. Hardware is to Set a READ Protect violation bit, and create an interrupt to the TMS9995.

3.5 INTERRUPT OPERATION

If any of the Protect conditions is violated, an interrupt is to be presented to the TMS9995. This signal is to be open drain or equivalent, and is to be active LOW.

The TMS9995 shall be able to sense the status of the three possible protect violations by performimg a MOVE BYTE operation from >8810 if CRUS is HIGH, or from >F870 if CRUS is LOW. Upon completion of this sense, the active status of the bit(s) shall be reset such that this operation does not preclude setting of a bit on the next PAS Memory access.

3.6 LAS OPERATION

The Mapper chip shall determine by sensing a single input pin, and logically ORing it with the internal SRAM Chip Select to determine if a PAS memory cycle is to occur. The external input is termed LASREQ*, and is LOW to indicate that the current memory cycle is for a LAS based device. The Mapper logic is to drive this line LOW when the SRAM is chip selected, including Direct Memory Access (DMA) loading and saving of the Mapper base registers.

3.7 MAPPER CONTROL OF CPU READY

The Mapper is responsible for passing through System READY to the TMS9995 for non PAS memory operations as well as controlling the TMS9995 READY for PAS memory operations.

3.8 MAPPER ADDRESS MUX FORMAT

The Mapper shall present to the user on the PAS Address Bus a 16-bit quantity after the TMS9995 MEMEN* occurs, but before PMEMEN* occurs, that is formatted such that the MSB is the WRITE Protect bit, the next lower bit is the EXECUTE Protect bit, the next lower is the READ Protect bit, the next five lower shall be zeros, and the lowest eight bits shall be the Most Significant eight bits of the 24-bit PAS. The Control signal MSAST* shall occur to indicate that this 16-bit quantity is stable on the address bus. The data shall be stable on the falling edge of MSAST*, but does not have to be stable on the rising edge.

The second 16-bit quantity associated with the PAS Address bus is the Least Significant 16 bits of the PAS Memory Cycle, and this must be stable prior to the time PMEMEN* goes active LOW. It must remain stable for the time period that PMEMEN* is LOW.

3.9 SRAM CONTROL FOR LOAD AND SAVE OPERATIONS

The Mapper shall control both the SRAM Chip Select and WE/CRUCLK* during DMA operations such that no CRU Clocks are generated. EARLY WRITE shall be the operation of the SRAM.

3.10 ADDITIONAL FEATURES

Additional features are included in the mapper in an effort to eliminate discrete logic on the TI 99/8.

3.10.1 SRAM Control. Decoding shall be included to control the 2K BYTE SRAM organized in the LAS of the TI 99/8. This SRAM shall be controlled by both the TMS9995 and the Mapper for LOAD/SAVE operations. The response equations for TMS9995 access are as follows for LAS TMS9995 based signals.

(CRUS)(LMEMEN)(LDBIN + LWE)(LA0)(LA1*)(LA2*)(LA3*)(LA4*) +

(CRUS*)(LMEMEN)(LDBIN + LWE)(LA0)(LA1)(LA2)(LA3)(LA4*)

3.10.2 64K BYTE DRAM Control. Decoding shall be included to generate a select signal to indicate that the PAS Memory Cycle in progress is within the PAS space of >00XXXX. The equation for this PAS decode is as follows.

(PMEMEN)(PA0*)(PA1*)(PA2*)(PA3*)(PA4*)(PA5*)(PA6*)(PA7*)

3.10.3 Speech Synthesizer Clock. The Mapper shall generate a clock that is the System Clock (10.73 MHz) divided by 33. The duty cycle of this free running clock shall be 16/33 - 17/33.

3.11 OUTPUT DRIVE CAPABILITY

Each output shall conform to the following DC drive capabilities.

PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
HIGH LEVEL OUTPUT VOLTAGE	VCC=MIN, IOH=MAX	2.4		V
LOW LEVEL OUTPUT VOLTAGE	VCC=MIN, IOL=MAX		.4	V
HIGH LEVEL OUTPUT CURRENT	VCC=MIN, VOH=2.4 V	100		uA
LOW LEVEL OUTPUT CURRENT	VCC=MIN, VOL=0.4 V	2		mA
OFF STATE OUTPUT CURRENT	VCC=MAX ! VO=2.4 V		20	uA
	! VO=0.4 V		-20	uA
OUTPUT CAPACITANCE	f=1MHZ, ALL OTHER PINS=0 V		15	pF

3.12 INPUT SPECIFICATIONS

INPUTS SHALL BE TTL COMPATIBLE.

3.13 PROPOGATION DELAYS

* ADDRESS PASS THRU
* PH3* CLOCK
* PMEMEN* SKEW
* PWE* SKEW

3.14 TESTING

Logic shall be included to facilitate testing of the Mapper chip. This logic shall include a sequential logic reset.

3.15 POWER UP OPERATION

One dummy PAS memory cycle shall be allowed to initilaize any sequential logic on the chip as deemed necessary. This is to be considedred as an undesirable feature, and no initialization should be a goal.

3.16 PINOUT DEFINITION

The signals of the Mapper chip shall be defined as follows.

MNEMONIC	TYPE	FUNCTION	PIN#
SCLK	IN	10.7 MHz SYSTEM CLOCK	36
CLKOUT	IN	2.68 MHz TMS9995 OUTPUT CLOCK	34
MEMEN*	IN	ACTIVE LOW TMS9995 MEMORY ENABLE	19
WE/CRUCLK*	IN	ACTIVE LOW TMS9995 MEMORY WRITE/CRU CLOCK	20
CRUS	IN	CONTROL SIGNAL TO CHANGE BASE OF SRAM	38
SRDY	IN	SYSTEM READY, LOW=NOT READY	41
DBIN*	IN	TMS9995 DBIN* OUTPUT (LAS DBIN)	22
IAQ/HDA	IN	TMS9995 IAQ/HOLDA OUTPUT	23
LASCS*	BIDI	ACTIVE LOW INDICATOR TO THE MAPPER INDICATING A LAS MEMORY CYCLE	37
A00 THRU A15/COUT	BIDI	TMS9995 ADDRESS BUS (LAS ADDRESS)	A00=17 A15=2
D0 THRU D7	BIDI	TMS9995 DATA BUS	D0=24 D7=31
PH3*	OUT	GENERATED 25% DUTY CY PH3* CLOCK	47
CPURY	OUT	GENERATED TMS9995 READY STATUS	18
PMEMEN*	OUT	GENERATED PAS MEMEORY ENABLE	46
PWE*	OUT	GENERATED PAS WRITE ENABLE	45
PDBIN	OUT	GENERATED PAS DATA BUS DIRECTION, HIGH LEVEL IS TMS9995 READ OPERATION	44
HOLD*	OUT	ACTIVE LOW HOLD REQUEST TO THE TMS9995	21
EXTINT*	OUT	ACTIVE LOW INTERRUPT REQUEST TO THE TMS9995	40

MNEMONIC	TYPE	FUNCTION	PIN#
MSAST*	OUT	ACTIVE LOW MOST SIGNIFICANT ADDRESS STABLE STROBE	43
PAS00 THRU PA15/COUT	OUT	PAS MULTIPLEXED ADDRESS BUS	PAS00=48 PAS15=63
SRAMCS*	OUT	ACTIVE LOW SRAM CHIP SELECT	39
SSRCLK	OUT	SPEECH SYNTHESIZER CLOCK	35
SKDRCS*	OUT	CHIP SELECT FOR PAS >00XXXX	42
VCC		+5V SUPPLY TO CHIP	1,33
VSS		GROUND SUPPLY TO CHIP	32,64

SECTION 4

ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUMS

4.1.1 Storage. -40 to +100 deg C

4.1.2 Operating. 0 to +70 deg C

4.1.3 Characterization. All parameters of the Mapper shall be verified in a full characterization effort.

SECTION 5

MECHANICAL SPECIFICATIONS

To be added later, contains symbolization, vibration testing, package dimensions, etc.